CLAIMS:

1. Detection unit for recovering a binary sequence (b_k) from an analogue signal (Sread) representing a runlength limited sequence (a_k) including a preliminary detection module (34) for generating a preliminary binary signal (Sb1) from the analogue signal (Sread) and a correction module for generating a corrected binary signal (b_k) from the preliminary binary signal, the correction module comprising

- a delay line (36, 38) having a chain of delay elements, coupled to the preliminary detection module (34),
- storage means (40, 42) for storing one or more first binary patterns and one or more second binary patterns for each of the first binary patterns,
- a comparator (44) coupled to the delay line (36) and the storage means (40), for outputting a detection signal (Sdet) indicating whether a sequence of bits present in the preliminary binary signal (Sb1) is identical to a first binary pattern,
- an evaluator (46) coupled to the storage means (40, 42) and to the input (30) for computing an evaluation value (Eval) indicating the likelihood that a binary pattern corresponds to the runlength limited sequence represented by the analogue signal (Sread),
- a selector (50) for selecting a binary pattern from the first binary pattern and the one or more second binary patterns for said first binary pattern having the highest likelihood,
- a corrector (50) for correcting the sequence of bits in the delay line (38) such that it corresponds to the selected binary pattern, if said selected binary pattern is not the first binary pattern,

an output (52) coupled to the delayline (38).

2. Detector according to claim 1, characterized in that the first binary pattern and the one or more second binary patterns differ at one bit, which bit is positioned at the edge of a run in the second binary pattern having a length greater than the minimum allowed runlength.

3. Detector according to claim 2, characterized in that the preliminary detection module (34) comprises,

- a slicer (34.1) coupled to the input,
- a runlength pushback detector (34.2) coupled to the output of the slicer (34.1),
- a shift detector (34.3) coupled to the output of the runlength pushback detector (34.2) which detects timeshifted runs having a length corresponding to the minimum runlength.

4. Detector according to claim 1, characterized in that the likelihood for a particular binary sequence is calculated from the difference between a value (Aact) of the analogue signal and a reference level (Aref).

5. Detector according to claim 4, characterized in that the reference level (Aref) is computed from said binary sequence with a finite length channel model representing the optical impulse response.

6. Detector according to claim 4, characterized in that the reference level (Aref) corresponding to a particular binary sequence is computed by measuring an amplitude value of the analog input signal during a plurality of occurrences of a particular binary sequence and averaging said amplitude values.

Sub a1

7. Device for reproducing an information carrier comprising a read head for reproducing a read signal (Sread) from a physically detectable pattern in tracks at the information carrier, movement means (3) for causing a relative movement between the information carrier (1) and the read head (2), a detector according to one or more of the claims 1 to 6 for reproducing a binary signal from the read signal, a first circuitry module (8.2) for controlling the movement means, a second circuitry module (12,13,16,10) for generating an output information signal (Sout) from the binary signal by channel decoding and/or error correction decoding.

8. Method for recovering a binary sequence (b_k) from an analogue signal representing a runlength limited sequence (a_k), the method comprising

- generating a preliminary binary signal from the analogue signal (S4),

- comparing a sequence of bits present in the preliminary with a first binary pattern (S5),
- if the comparison has a positive result for a first binary pattern computing an evaluation value for said first binary pattern and for one or more second binary patterns, the evaluation value indicating the likelihood that a binary pattern corresponds to the runlength limited sequence represented by the analogue signal (S6),
- selecting a binary pattern from the first binary pattern and the one or more second binary patterns for said first binary pattern which has the highest likelihood (S7),
- correcting the sequence of bits in the preliminary binary signal such that it corresponds to the selected binary pattern, if said selected binary pattern is not the first binary pattern (S7).

9. The method according to claim 8 characterized in that
- the first binary pattern and the one or more second binary patterns differ at exactly one bit, which bit is positioned at the edge of a run in the second binary pattern having a length greater than the minimum allowed runlength.